(IJIASE) 2018, Vol. No. 4, Jan-Dec **e-ISSN: 2454-9258, p-ISSN: 2454-809X**

EMPLOYABILITY OF DIGITAL IMAGE PROCESSING APPLICATION IN FPGA AND ASIC IMPLEMENTATION OF SYSTOLIC ARRAYS FOR THE DESIGN OF OPTIMIZED MEDIAN FILTER

Anoushka Gupta

ABSTRACT

Background/Objectives*: A new systolic algorithm for median filtering is analyzed in this paper; this algorithm is suitable for VLSI implementation to design an optimized median filter.* ***Methods/Statistical analysis:*** *The modified sort algorithm avoiding the main problem of the median filter is its high computational cost (for sorting N pixels, the temporal complexity is O (N·log N), even with the most efficient sorting algorithms, the clock cycle time is equal to the propagation delay of a simple comparator circuit.* ***Results/Findings****: The hardware requirements of the architecture are significantly lower than those of previously reported systolic array architectures. An implementation of an 8-bit word length 3X3 window size filter in an ALTERA EP1C3T100C6 FPGA achieved a clock rate in excess of 197 MHz with 85 cells only.* ***Conclusion/Application:*** *An improved algorithm has been proposed to address the problem of a median filter that is high computation time is encountered.*

1. INTRODUCTION

DIP is the utilization of PC calculations to perform picture preparing on advanced pictures. It permits a lot more extensive scope of calculations to be applied to the info information and can keep away from issues, for example, the development of clamor and sign contortion during handling. A few decades ago, image processing was done largely in the analog domain, chiefly by optical devices. These optical methods are still essential to applications such as holography because they are inherently parallel; however, due to the significant increase in computer speed, these techniques are increasingly being replaced by digital image processing methods10.

During the transmissions of pictures over channels, pictures are frequently tainted by drive clamor because of defective correspondence or boisterous channels. Such clamours might be acquainted due to a broken camera or something like that. In a high contrast digitized picture, pixels debased by positive driving forces show up as white specks, and those adulterated by negative motivations show up as dark dots. Clamour might be brought about by different sources, for example, varieties in locator affectability, natural varieties, and transmission or quantization blunders. Clamour motivations can be negative or positive. Scaling, as a rule, is a piece of the picture digitizing process. Since motivation defilement more often than not is huge contrasted and the quality of the picture signal, drive clamor is, for the most part, is digitized as extraordinary (unadulterated dark r white)

values in a picture. Therefore, the negative drive shows up as dark (pepper) focuses on a picture, and positive motivations show up as white (salt) focuses on the image.

1.1 Introduction to WaveFront and Systolic Architectures

The original, still broadly utilized, of advanced control frameworks executions depend on the single universally useful processor engineering emerging from the von Neumann model. Further, the advancement of these frameworks, estimated as far as expanded speed and improved execution, has been verifiably connected to advancements in registering innovation. This has prompted the utilization of specific reason computerized signal processors and, hence, control-devoted 'advanced control processors,' the two of which utilize the uniprocessor architecture7,8.

Fast advancements in Very Large Scale Integration (VLSI) circuit innovation presently license the creation of different Processing Elements (PEs) onto a solitary silicon chip9. This, thusly, has prompted the advancement of structures as systolic and wavefront clusters, which have been the subject of escalated inquire about, roused by various computationally concentrated applications regions.

As a result, a systolic exhibit is a system of processors that musically figures and goes information through the system. Its significant highlights are measured quality and normality n terms of VLSI usage, direct rate pipeline ability, spatial and worldly territory, information contribution to the exhibit just pipelined through limit PEs, and synchrony of information stream and calculation.

A wavefront cluster has a similar design; however, here, the control of information stream and calculation is self-coordinated and information-driven instead of constrained by a synchronized worldwide clock.

1.2 Cascaded Decision-Based MedianFilter

This architecture uses a combination of both Decision-based Median Filter (DMF) and Unsymmetrical Trimmed Midpoint Filter (UTMF), in a cascaded connection shown in Figure 1. The noisy image is first processed using the Decision-based median filter. The output of DMF is given as the input to the UTMF.

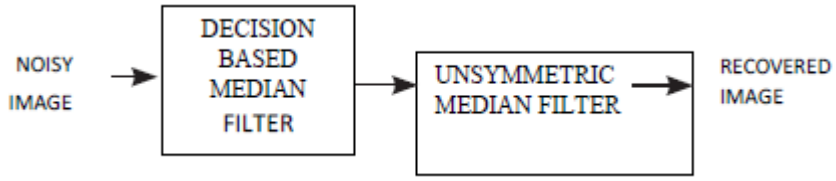

Figure 1. Cascaded Filter

(IJIASE) 2018, Vol. No. 4, Jan-Dec **e-ISSN: 2454-9258, p-ISSN: 2454-809X**

2. PROPOSED ARCHITECTURE

The proposed architecture is an extension of the general median filter. It actually renders all the positive features of these algorithms and overrides their frailties with their capabilities. The efficient algorithm requires much lesser logic cells and runs at amazing speed when compared to the conventional ones.

The proposed architecture takes the noisy image as input, from the noisy image, a 3x3 window is selected with the center pixel as reference. The reference pixel i.e., the center pixel, is checked whether it is a noise. If it is not a noise, then no operation is performed on the pixel, the same pixel value is retained at the output. If the reference pixel is noise, then the median is found using carry logic sorting; the median value found is checked whether it is a noise. If the median is not a noise, then the median value is placed in the output. If the median is found to be noise, then the left neighborhood adjacent element value is placed in the output. This procedure is repeated with all pixels in the input as reference pixels. The output obtained will be noise-free and also less blurred. And the edge-preserving of the property of the median filter is also retained. For median computing values of the window, modified shear sorting algorithm is used due to its simplicity and efficiency. Presently the principal component of the window is the base worth, the last component of the window is the most extreme worth, and a central component of the window is the middle worth.As seen above, after the computation of median for the elements in the window at a particular position, the center element of the window is checked for its nature, i.e., whether it is the original pixel value or the noise value. Then the center element of the window considered is replaced with the corresponding value as in (cases 1, 2, and 3). Subsequently, the window moves toward the right for a new set of window values, and this processing, as well as updating procedure, goes on and on until the end of the image elements are reached.

(IJIASE) 2018, Vol. No. 4, Jan-Dec **e-ISSN: 2454-9258, p-ISSN: 2454-809X**

2.1 Algorithm

Step 1: Read the noisy image

Step 2: Select a window of size (3X3) with pixel to be processed P(X, Y) as centre pixel.

Step 3: Get the pixels from the window.

Step 4: Sort the pixel's values.

Step 5: case 1: If P (X, Y) > min(window) and P (X, Y) < max(window) then P (X, Y) is an uncorrupted pixel so it is used as it is and placed in output image O (X,Y), O(X,Y)=P(X,Y)

Else

P (X, Y) is corrupted pixel (go to step 6).

Step 6: case 2: Check If (median(window)>min(window) and median(window) < max(window)) then place the median(window) in the corresponding location of original pixel P (X, Y) in output matrix O (X, Y). O (X, Y) =median(window)

Else

case 3: median (window) is a noise, so place the processed neighbourhood pixel O (X, Y-1) value in the output matrix O (X, Y). O (X, Y) =O (X, Y-1)

Where,

P (X, Y) input matrix

O (X, Y) output matrix

2.2 Flow Chart for Proposed Architecture

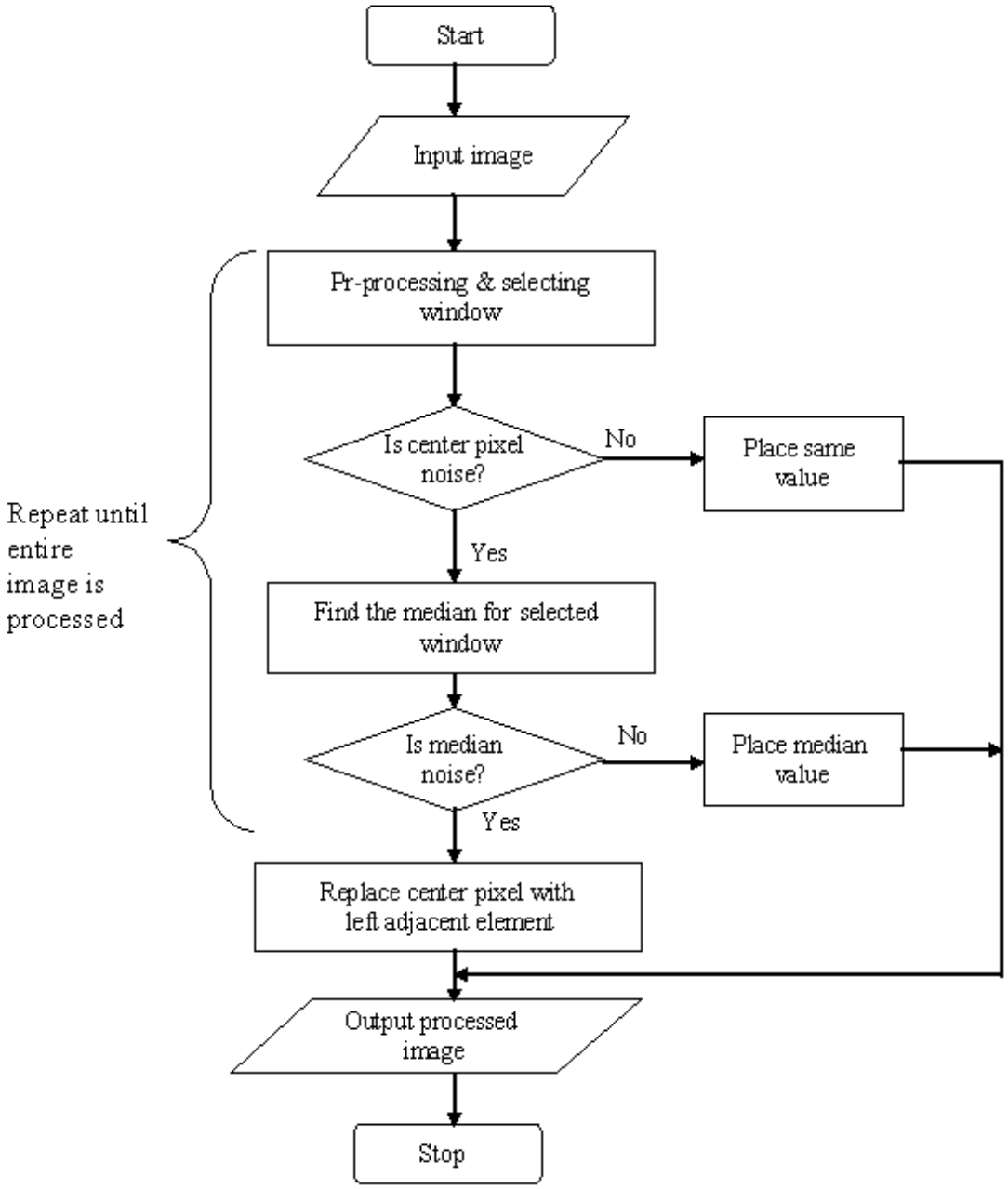

Figure 2. Flow chart for the proposed architecture.

3. RESULT

Median blocks of the carry logic and shear sorter architectures are designed and simulated in Altera version 4.1 Compiler. The developed shear sorter design uses parallel architecture. Three Cell Sorter block takes only three inputs at a time and arranges them in the ascending order. Seven such TCSs are used in the median block to find the median. Therefore, the block processes the input values in

a parallel manner. In the carry logic sorter, the nine input values of the considered matrix are sorted and compared, and the median is obtained. This median block is used in the decision block, which checks the conditions for noise-free pixels, and the final output is obtained. The results show that is architecture developed is simple, and it is very fast in computing the output.

3.1 Simulation Result

The developed VHDL codes for carrying logic sorter and shear sorter architectures are simulated using Xilinx version 7.1, and the synthesis report is obtained using Altera Version 4.1, and the total number of logic cells in both the architectures is compared.

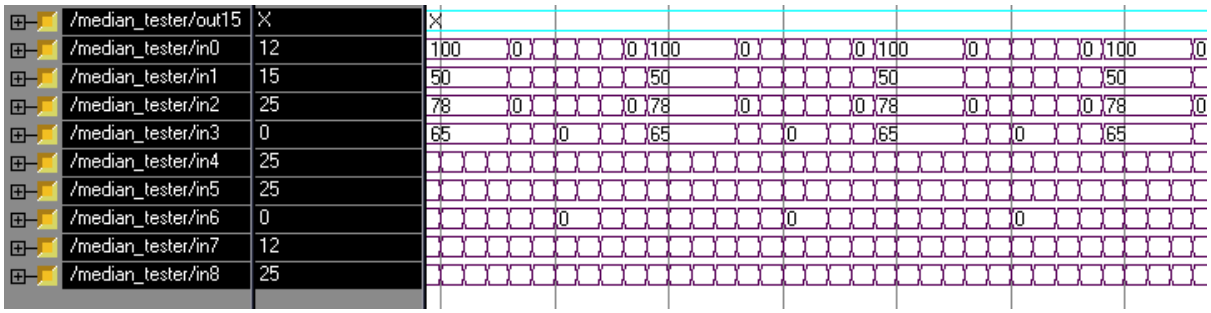

Figure 3. The output waveform of carrying shear sorter.

3.3 Output Waveform of carrying Logic Sorter

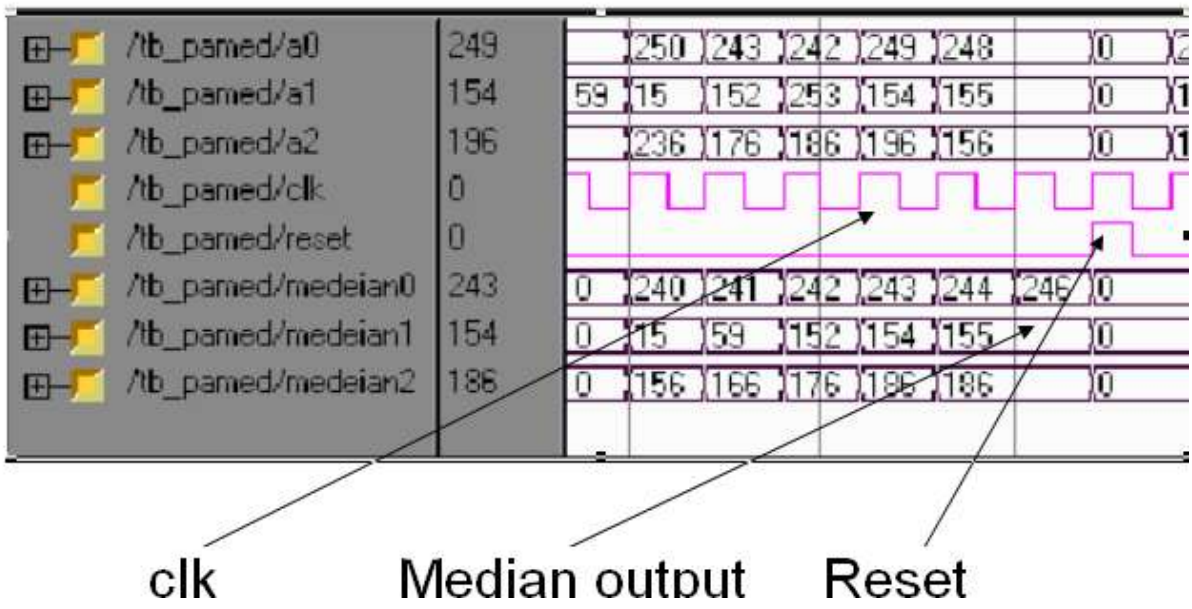

Figure 4. Output Waveform of carrying Logic Sorter.

(IJIASE) 2018, Vol. No. 4, Jan-Dec **e-ISSN: 2454-9258, p-ISSN: 2454-809X**

4. CONCLUSION

This paper presents the data dependence analysis of the insert sort algorithm of the median filter from which a novel word-level algorithm with good data dependence was proposed. In the modified algorithm, the operations which compare and insert with high-speed throw combined into a single stage. Furthermore, the data dependence within the five stages is simplified by a looking forward method, and the clock cycle time is reduced to the propagation delay of a simple comparator circuit. The top module of this algorithm has synthesized throw ALTERA EP1C3T100C6 FPGA achieved a clock rate in excess of 197 MHz. The area is 85 Cells, which lower than the other existing algorithms.

An improved algorithm has been proposed to address the problem of a median filter that is high computation time is encountered.